I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on.

10/7/03
Date of Deposit

Pamela J. Squyres
Name (printed)

Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Shuo Gu et al. Application No.: Filed: Herewith Title: Uniform Seeding to Control Grain and Defect Density of Crystallized Silicon for Use in Sub-Micron Thin Film Transistors Attorney Docket No.: MA-108	Group Art Unit: Unknown Examiner: Unassigned

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

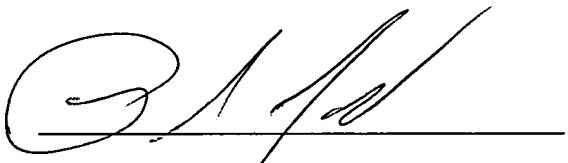
Dear Sir or Madam,

Pursuant to the obligation under 37 CFR § 1.56 and in conformance with 37 CFR §§ 1.97-1.99, Applicants hereby submit documents A1-A12 listed on the attached form PTO-1449 for consideration by the Examiner. Copies of these documents are enclosed herewith. Applicants request that the Examiner review the entire disclosure of these documents and make them of record.

The filing of this Information Disclosure Statement does not constitute an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR §1.56(b). Further Applicants reserve the right to contest that any of the information submitted herewith is prior art against the present application.

Dated: October 7, 2003

Respectfully submitted,



Pamela J. Squyres
Agent for Applicants
Reg. No. 52,246

Pamela J. Squyres
Matrix Semiconductor
3230 Scott Blvd
Santa Clara, CA 95054
Tel. 408-869-2921

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Applicati n Numb r	Unknown
Filing Dat	Even Date Herewith
First Named Inv nt r	Gu, Shuo
Gr up Art Unit	Unknown
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: MA-108

US PATENT DOCUMENTS

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	A1	5,821,152	10/13/1998	Han et al.			
	A2	5,923,968	07/13/1999	Yamazaki et al.			
	A3	6,146,966	11/14/2000	Hirota et al.			
	A4	6,204,156	03/20/2001	Ping			
	A5	US20020028541A1	03/07/2002	Lee et al.			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	A6	BANERJEE, ADITI.,et al. ,"Fabrication and Performance of Selective HSG Storage Cells for 256 Mb and 1Gb DRAM Applications", IEEE Transactions on Electron Devices, Vol.47, No.3, (3/2000),584-592	
	A7	BO, XIANG-ZHENG.,et al. ,"Spatially selective single-grain silicon films induced by hydrogen plasma seeding", J. Vac. Sci. Technol. B 20(3), (May/Jun 2002),	
	A8	DAHLHEIMER, C..E. ,et al. ,"Laser-Interference Crystallization of Amorphous Silicon", 54-55	
	A9	OH, CHANG-HO.,et al. ,"A Proposed Single Grain-Boundry Thin-Film Transistor", IEEE Electron Device Letters, Vol.22, No.1, (1/01),20-22	
	A10	SONG, I.H. ,et al. ,"A New Multi-Channel Dual-Gate Poly-Si TFT Employing Excimer Laser Annealing Recrystallization on pre-patterned a-Si thin Film", 0-7803-7463-X02 (C) 2002 IEEE, (2002),	
	A11	SUBRAMANIAN, VIVEK.,et al. ,"Controlled Two-Step Solid-Phase Crystallization for High-Performance Polysilicon TFTs", IEEE Electron Device Letters Volume: 18 Issue: 8 , Aug 1997, (1997),378 -381	
	A12	YAMAUCHI, N.,et al. ,"Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: Theory, experiments, and thin-film transistor applications", Journal of Applied Physics, vol. 75, (1994),3235-3257	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached